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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,988	08/15/2001	Jun Koyama	740756-2348	8058

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EXAMINER	
NGUYEN, CHANH DUY	
ART UNIT	**PAPER NUMBER**
2675	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,988	KOYAMA ET AL.	
	Examiner	Art Unit	
	Chanh Nguyen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-29* is/are pending in the application.

4a) Of the above claim(s) *7-9,13 and 16-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 10, 12, 14, 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on January 27, 2005 have been entered and considered by examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by applicant's admitted prior art (Figures 5-6 and 12B).

Applicant's admitted prior art (Figures 5-6 and 12B) discloses the most closely resembling the subject mater of the claims including thin film transistor, clock lines, two layer structures and the lower layer extends in a same direction as the upper layer as recited in the claims. That is Figures 5A-5B show the a driving circuit TFT (which includes clock input terminals 208-209 in Figure 2 as well as clock input terminals 501-509 in Figure 6) formed in the same layers structure as a pixel TFT which includes gate, drain source (Figure 5B). Figure 6 further describes that "in the a driving circuit of a conventional liquid crystal display device, where clock wiring lines, video signal wiring lines, and control wiring lines of a shift register are formed, those wiring lines are formed at the same time a source and drain electrodes of a thin film transistor" (see page 5 line 24 through page 6, line 10 of the specification). Figures 4A- 4D clearly

show at least two layers structure for forming source/drain and gate line electrodes. Figure 5A-5B show the wiring lines including clock lines (driver circuit TFT) associated with layers structure of source/drain gate line electrodes (i.e. pixel TFT). Furthermore, Figure 12B details of Figures 5A-5B how the clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. For example, the clock wiring lines are made of two layers: a lower layer (1114) is a gate electrode and an upper layer (1111, 1112) is a source and drain electrode. The lower layer (gate 1114) extends in a direction as the upper layer (see Fig. 12B).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 10, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art admitted by applicant in view of Mitra (U.S. Patent No. 5,994,765).

As to claim 10, note the discussion of prior art above, prior art admitted by applicant discloses a semiconductor as recited in claim 10 with exception that the prior art does not mention shielding line. Mitra teaches a well-known shielding line (103) disposed on interval between the clock lines (101). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used shielding line as taught by Mitra to the semiconductor of the prior art so as to help prevent clock signals propagated on the clock line from electromagnetically coupling with other signal lines (see column 2, lines 18-22 of Mitra).

As to claims 12 and 14-15, the limitations recited in these claims are met by the prior art admitted by applicant (Figures 5-6 and 12B).

7. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior art admitted by Applicant in view of Yamazaki (U.S. Patent No. 6,175,395 B1).

As to claim 5, Applicant's admitted prior art discloses a semiconductor device including a substrate having at least one driving circuit (see Fig 5B; driver circuit TFT) comprising a plurality of thin film transistors pixel TFT, and clock lines (501-506) for

supplying clock signals to the driving circuit , and wiring lines crossing the clock lines (see Figure 6). Applicant's admitted prior art does not mention black matrices over the thin film transistors. Yamazaki teaches a black matrix formed over the driver circuit region wherein said wiring lines comprises the same layer as the black matrices (see column 2, lines 23-25,lines 63-65, column 3, lines 24-25). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used the black matrix as taught by Yamazaki to on the driving circuit wiring of prior art admitted by applicant since the black matrix can of Yamazaki can shield the light for both driving circuit and driver circuits (see column 2,lines 38-50 of Yamazaki).

As to claim 6, Applicant's admitted prior art clearly teaches each of clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors wherein the lower layer extends in a same direction as the upper layer. That is Figures 5A-5B show the a driving circuit TFT (which includes clock input terminals 208-209 in Figure 2 as well as clock input terminals 501-509 in Figure 6) formed in the same layers structure as a pixel TFT which includes gate, drain source (Figure 5B). Figure 6 further describes that "in the a driving circuit of a conventional liquid crystal display device, where clock wiring lines, video signal wiring lines, and control wiring lines of a shift register are formed, those wiring lines are formed at the same time a source and drain electrodes of a thin film transistor" (see page 5 line 24 through page 6, line 10 of the

specification). Figures 4A- 4D clearly show at least two layers structure for forming source/drain and gate line electrodes. Figure 5A-5B show the wiring lines including clock lines (driver circuit TFT) associated with layers structure of source/drain gate line electrodes (i.e. pixel TFT). Furthermore, Figure 12B details of Figures 5A-5B how the clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. For example, the clock wiring lines are made of two layers: a lower layer (1114) is a gate electrode and an upper layer (1111, 1112) is a source and drain electrode. The lower layer (gate 1114) extends in a direction as the upper layer (see Fig. 12B).

Response to Arguments

8. Applicant's arguments filed June 03, 2004 have been fully considered but they are not persuasive.

On page 7, last two paragraph, applicant argues that the Office Action has not established an anticipation rejection, Examiner disagree with applicant this point of view since the prior art (Figures 5 and 6) discloses the all the claimed limitation including thin film transistor, clock lines, two layer structures as recited in the claims.

On page 8, applicant argues that "Figures 5 and 6 do not teach that each of clock lines or each of base portions of the clock lines is made of a two layer structure, a lower

layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors".

Examiner disagrees with applicant and would like to present his point of view as follows:

First of all, Figures 5A-5B show the a driving circuit TFT (which includes clock input terminals 208-209 in Figure 2 as well as clock input terminals 501-509 in Figure 6) formed in the same layers structure as a pixel TFT which includes gate, drain source (Figure 5B). Figure 6 further describes that "in the a driving circuit of a conventional liquid crystal display device, where clock wiring lines, video signal wiring lines, and control wiring lines of a shift register are formed, those wiring lines are formed at the same time a source and drain electrodes of a thin film transistor" (see page 5 line 24 through page 6, line 10 of the specification). Figures 4A- 4D clearly show at least two layers structure for forming source/drain and gate line electrodes. Figure 5A-5B show the wiring lines including clock lines (driver circuit TFT) associated with layers structure of source/drain gate line electrodes (i.e. pixel TFT). Furthermore, Figure 12B details of Figures 5A-5B how the clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. For example, the clock wiring lines are made of two layers: a lower layer (1114) is a gate electrode and an upper layer (1111, 1112) is a source and drain electrode.

While this is unlike applicant's disclosed device (Figure 12A), it reads on broad claimed language.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chanh Nguyen whose telephone number is (571) 272-7772. The examiner can normally be reached on Monday- Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CN
C. Nguyen
April 15, 2005

Chanh Nguyen
Primary Examiner
Art Unit 2675